Canon

MDD-210

FLOPPY DISK

TECHNICAL GUIDE

1983 JUNE

P/N : K-61222-03

1. Specifications

1.1 Basic specifications

	MDD210	
	Single density	Double density
Storage capacity (per disk)	250 KB	500 KB
(per track)	3.125 KB	6.25 KB
Transfer rate	125 K-bits/sec	250 K-bits/sec
Average latency time	100 ms	
Access time	-	
Track-to-track positioning time	6 ms max	
Average access time	200 ms max	
Head loading time	30 ms max	
Head settling time	30 ms max	
Motor start time	1 sec max	

1.2 Physical specifications

	MDD210	
	Single density	Double density
Innermost circumference recording density	2938 BPI	5876 BPI
Number of tracks	80 (both sides)	
Track density	48 T.P.I	
Track radius	Outer circumference 57.15 Inner circumference 34.4	
Modulation system	FM or MFM	

1.3 Environmental conditions

Ambient temperature in operation	5° - 45°C
Ambient temperature in transportation	-40° - 62°C
Temperature in non-operation	-22° - 55°C
Relative humidity	20% - 80% RH
Max wet bulb temperature	29°C

1.4 Power supply

+5V ± 5% Ripple 50 mVp-p	TYP 0.7A MAX 1.0A
+12V ± 5% Ripple 100 mVp-p	TYP 0.9A MAX 1.6A

1.5 Dimensions

Width	146.1 mm
Height	57.5 mm
Depth	196.5 mm
Weight	1.3 kg

1.6 Reliability

M.T.B.F.	10000 P.O.H.
Unit life time	5 years
M.T.T.R.	30 minutes
Error rate	
Soft read error	10^{-9} bits
Hard read error	10^{-12} bits
Seek error	10^{-6} seeks

1.7 Vibration & impulse

Resistance against vibration in operation	Acceleration	1G
	Vibration sweep	5 - 100 Hz
	Vibration direction	X.Y.Z. directions
Resistance against vibration in transportation	Acceleration	2G
	Vibration sweep	5 - 100 Hz
	Vibration direction	X.Y.Z. directions
Resistance against impulse in transportation	To satisfy all specifications after being dropped from height of 50 cm in a packed condition.	

2. Interface

The MDD interface consists of two sections.

1. Signal
2. Power supply

Each line is detailed below.

2.1 Signal interface

The daisy chain or radial chain is used for the signal interface of the select line, allowing connection to a maximum of 4 MDD's. In case of the daisy chain, only the last MDD is terminated. A resistance array close to the connector J1 is provided for this termination. In short, the termination is provided by the resistance array and select line. (The resistance array is removable.)

The assignment of the interface connector and power connector is shown below.

Signal connector

Ground return	Signal pin	Signal name	Ground return	Signal pin	Signal name
1	2		19	20	STEP
3	4	HEAD LOAD	21	22	WRITE DATA
5	6	SELECT 4	23	24	WRITE GATE
7	8	INDEX	25	26	TRACK 00
9	10	SELECT 1	27	28	WRITE PROTECT
11	12	SELECT 2	29	30	READ DATA
13	14	SELECT 3	31	32	SIDE SELECT
15	16	MOTOR-ON	33	34	READY
17	18	DIRECTION-IN			

Power supply

Pin No.	Power name
1	+12V DC
2	+12V GND
3	+5V GND
4	+5V DC

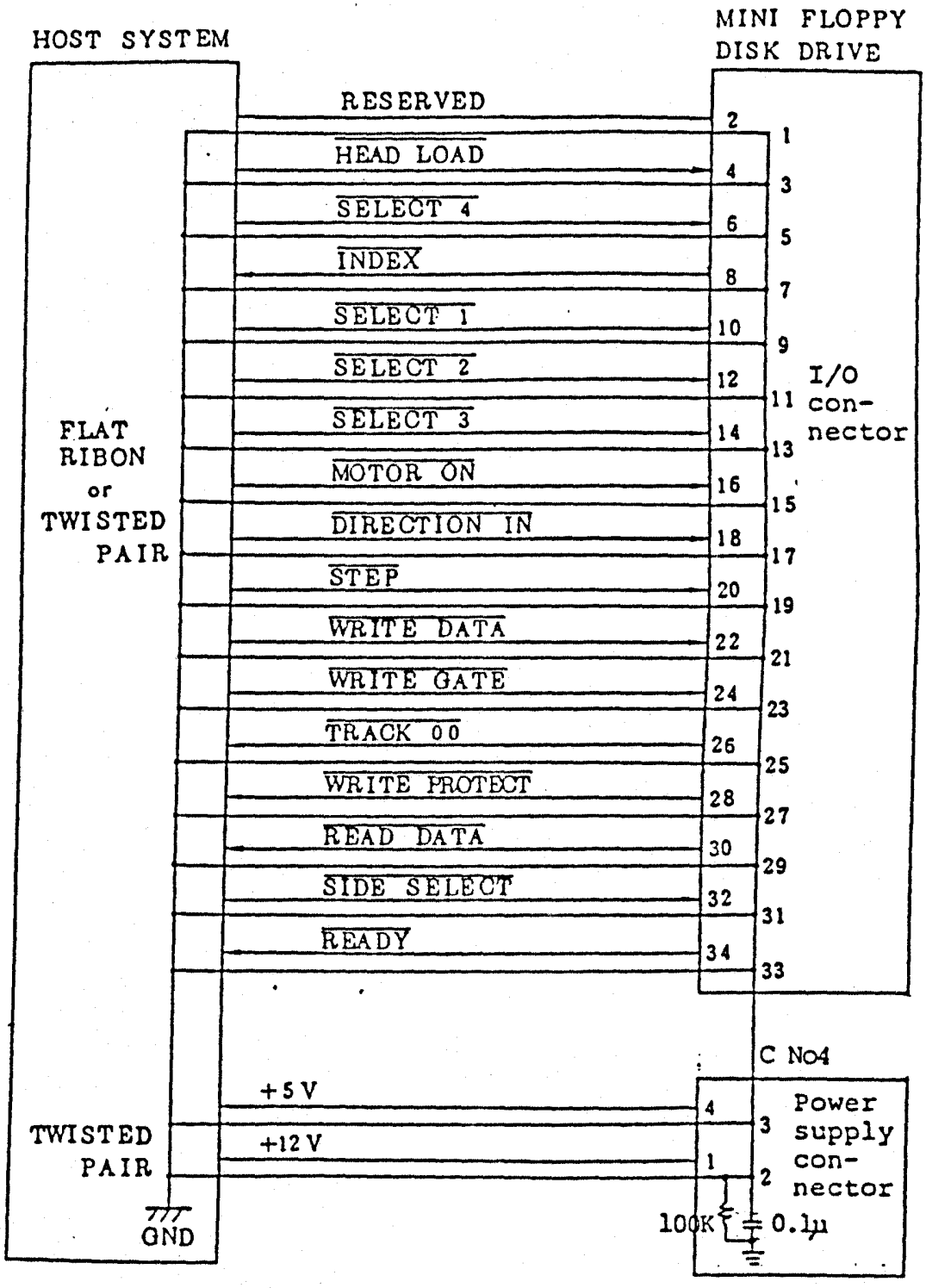


Fig. 2-1 Signal interface

2.2 Input line

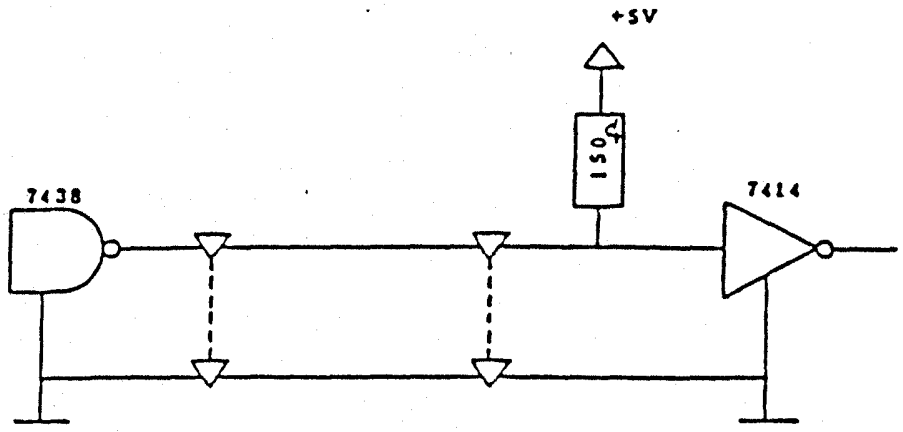


Fig. 2-2 Recommended 1/0 interface

Max cable length: 3m, Ribbon wire or twist pair wire
Signal interface specifications

Logical 0 = 0.0 - 0.8V (active)
Logical 1 = 2.0 - 5.25V (inactive)

(1) SELECT 1-4

A maximum of 4 MDD's can be connected in the daisy chain mode. The DIP switch is used to switch each drive. (All switches are set to select 1 at the factory.)

The select lines 1 - 4 are used to select the ranked MDD. Only the selected drive can send/receive signals.

(2) MOTOR-ON

This signal is a spindle motor-ON/OFF signal and the motor is turned ON at logical 0.

(3) DIRECTION-IN

The function of this signal is to determine the direction of the read/write head, and must be set at lease 1 μs earlier than the STEP pulse falling edge. The direction of the head carriage by the DIRECTION-IN signal is handled as follows.

Logical 1 = Inner direction from the disk center
Logical 0 = Central direction of the disk

(4) STEP

Sending the logical 0 pulse to this line causes the read/write head to move towards the direction determined by the DIRECTION-IN. In usual cases, this step speed is 3m sec/track.

When the write gate signal is logical 0, the STEP signal is inhibited. For details, see the timing chart (Fig. 2-6).

(5) WRITE GATE

This is a signal to control the write data and read data. The write data are valid at logical 0, and the read data are valid at logical 1.

In case of a write-protected disk, the write is inhibited within the drive. Another function of the write gate is to internally operate the tunnel erase, which keeps operating for 1200 μs after the write gate has been closed.

(6) WRITE DATA

This signal is used to write data into the disk. Power is supplied to the R/W head when logical 1 changes to logical 0, which causes a magnetic flux. This signal is valid when the WRITE GATE is logical 0.

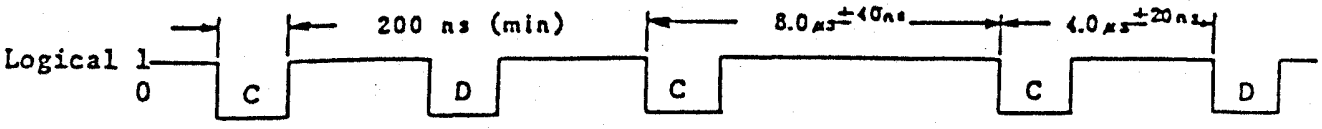


Fig. 2-3 WRITE DATA timing (FM)

(7) HEAD LOAD

When this signal becomes logical 0, the head is loaded and is released at logical 1. Depending on the DIP switch selection, both the HEAD LOAD and SELECT are available, or the head can be loaded by SELECT only. In every case, the head is loaded only when the READY signal is logical 0.

The function of this signal is to control the solenoid and operation confirmation LED. Any mode is selectable by the DIP switch.

When the IN-USE signal becomes logical 0, the door lock functions, making it impossible to take the disk out.

(8) SIDE SELECT

The function of this signal is to select the two R/W heads. Logical 0 selects head 1. When one head is switched to the other head, the 200 μs wait time at the read time and 1200 μs wait time at the write time are required respectively.

2.3 Output line

Five output lines are provided, the interface of which is shown in 2.1.

Logical 0 = 0.0 - 0.4V (active)
Logical 1 = 2.4 - 5.25V (inactive)

(1) READY

This signal is issued when the disk is inserted at the power-ON time, and is logical 0 at the normal select time. It is logical 1 in other cases.

(2) TRACK 00

This signal becomes logical 0 when the read/write head is positioned at track 00, and is used to detect the head carriage position after power-ON.
(When the TRACK 00 signal is logical 0, sending one additional step pulse towards the outer circumference causes TRACK 00 to be logical 1. Sending three additional step pulses towards the outer circumference causes TRACK 00 to return to logical 0.)

(3) INDEX

The MDD210 carries the index detection feature, and issues the detection signal when the index hole comes out.

Usually this signal is logical 1, and becomes logical 0 when the index hole comes out (1.5 - 5 m sec).

On the soft sector disk, a signal at one hole indicates the start of the track. When the disk is not inserted, the index signal remains at logical 0. Fig. 2.4 indicates the index timing.

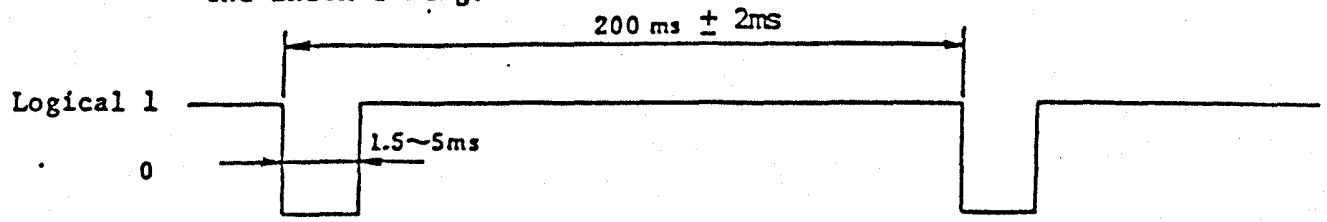


Fig. 2-4 Index timing

(4) READ DATA

The function of this signal is to output the raw data read by the read circuit of the MDD210. Usually this signal is logical 1 and becomes logical 0 when the magnetic inversion exists on the disk.

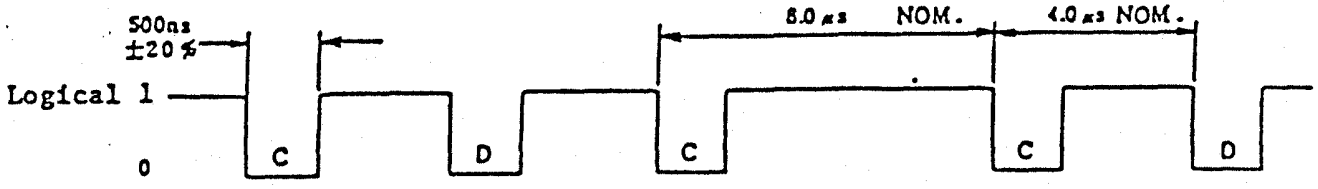


Fig. 2-5 READ DATA

(5) WRITE PROTECT

The function of this signal is to notify the host system that a write-protected disk has been inserted.

When the protected disk is inserted, the signal becomes logical 0, and the write into the disk is inhibited in the MDD. For write protect, the disk write prevention notch can be covered by an opaque label.

2.4 Jumper pin

As aforementioned, switching the DIP switch located on the PCB permits a desired function to be used.

The head load, operation confirmation LED and door lock solenoid can be controlled by DIP switches SW1 - SW3.

See Fig. 2-7 Block diagram.

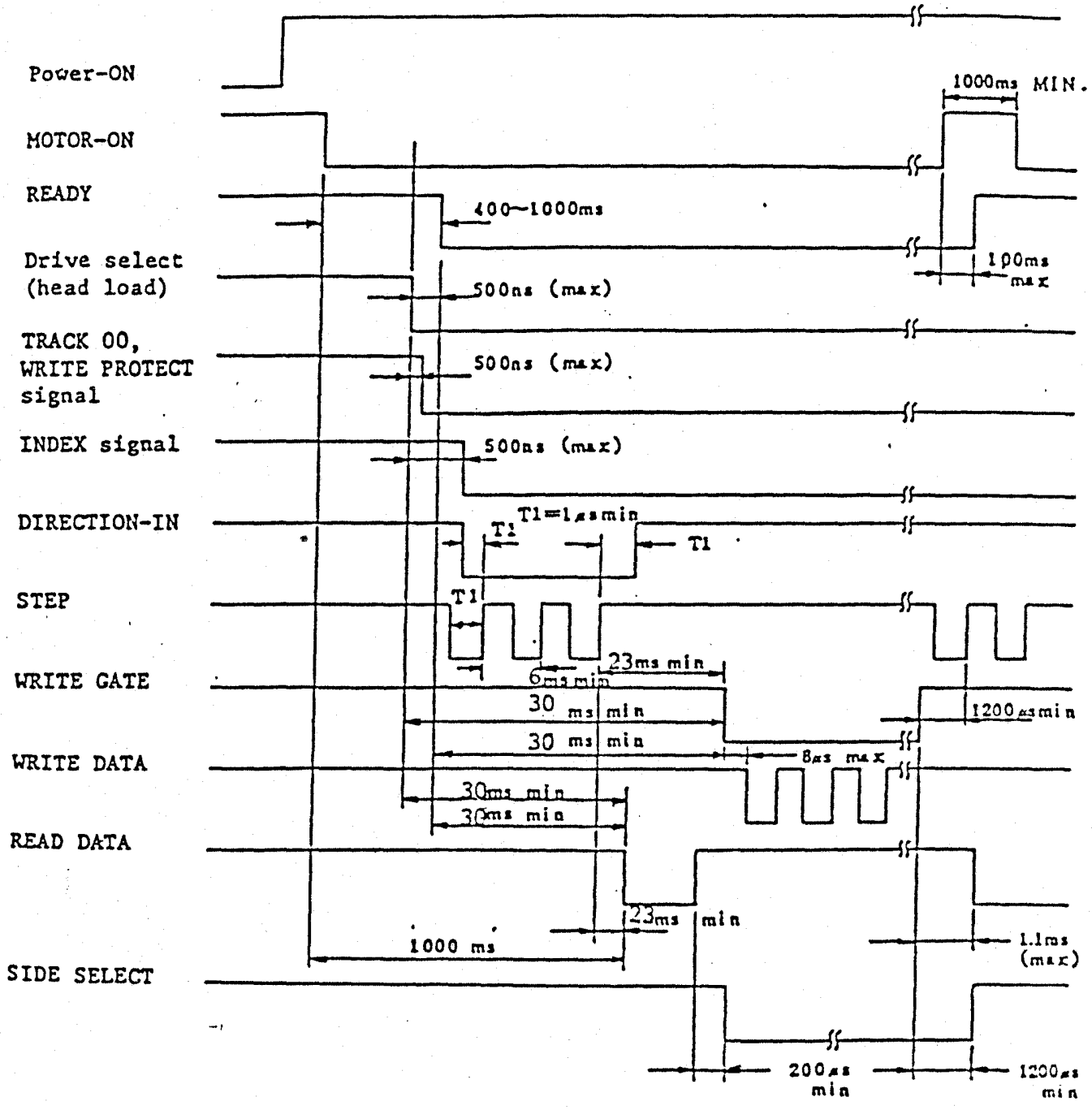
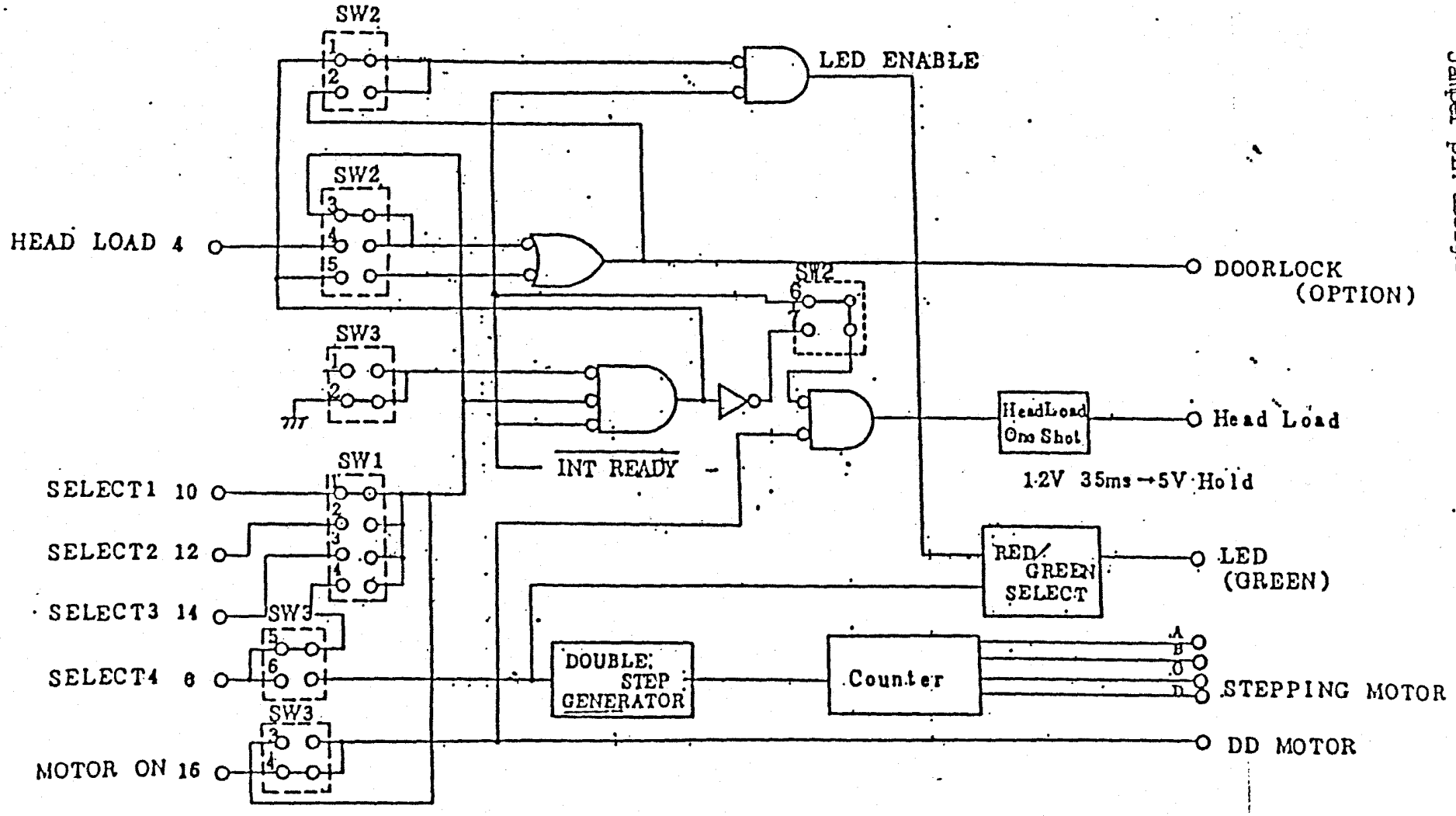


Fig. 2-6 Timing chart



Jamper pin assignment

Fig. 2 - 7

3. Operation

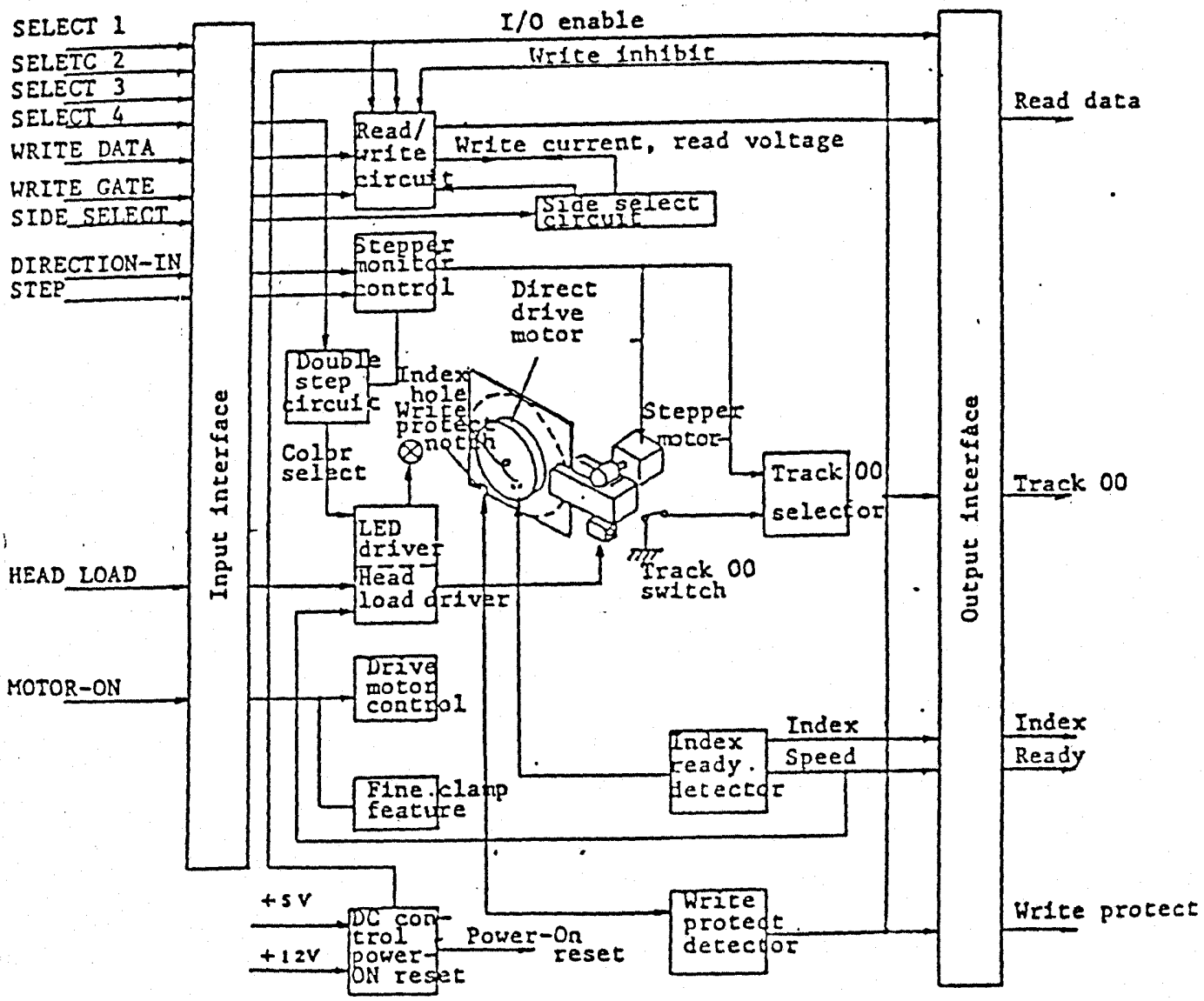
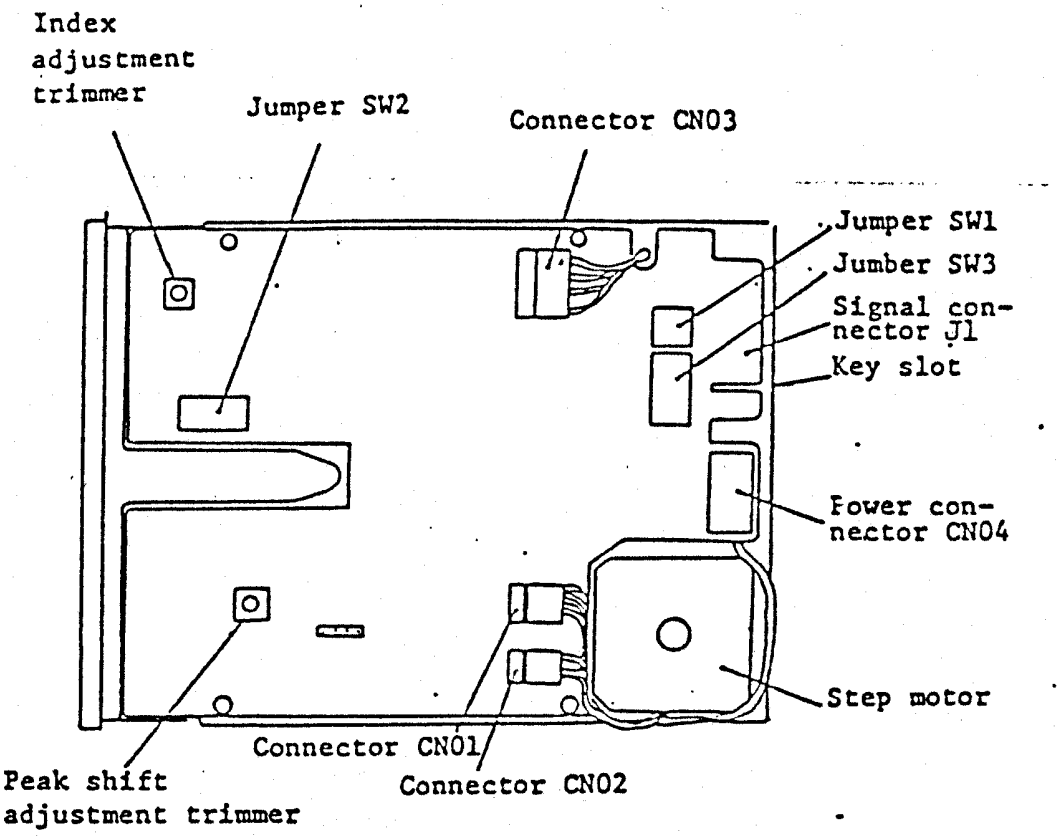
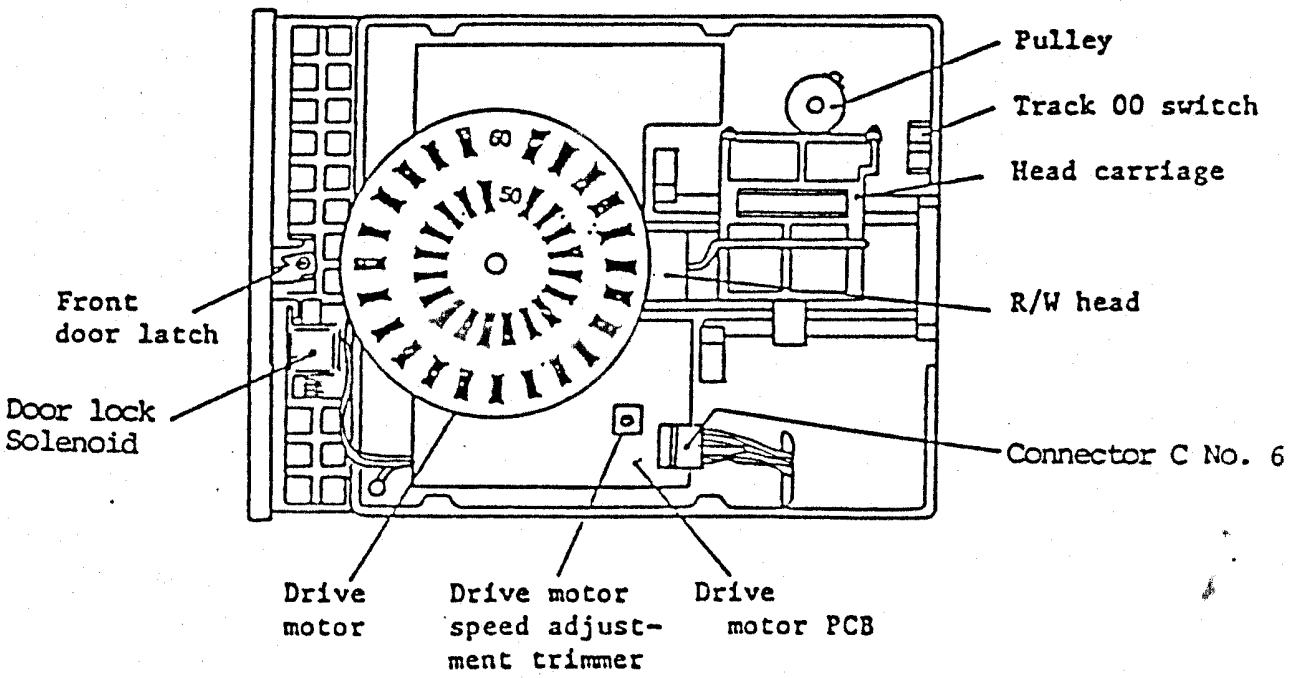


Fig. 3-1 Block diagram


Index adjustment trimmer
Jumper SW2
Connector CN03
Jumper SW1
Jumber SW3
Signal connector J1
Key slot
Power connector CN04
Step motor
Connector CN01
Connector CN02
Peak shift adjustment trimmer


Pulley
Track 00 switch
Head carriage
R/W head
Front door latch
Door lock Solenoid
Connector C No. 6
Drive motor
Drive motor speed adjustment trimmer
Drive motor PCB

3.1 Drive feature

The spindle of this drive is directly driven by the DC motor at a fixed speed of 300 rpm (200 ms/revolution). The drive motor starts and stops by the MOTOR-ON signal.

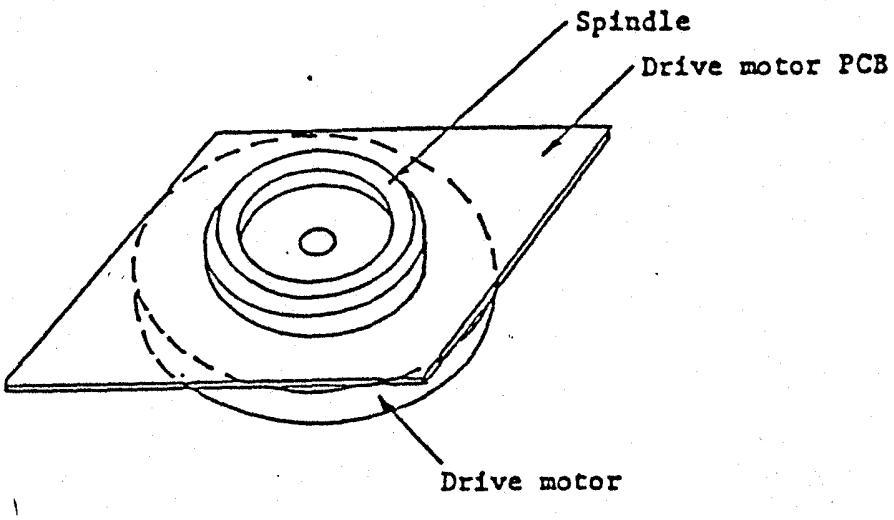


Fig. 3-2 Drive feature

3.2 Spindle front door feature

This feature consists of the following parts.

Spindle
Center cone
Cone thrust arm
Door latch
Front door

Inserting a disk and pressing the front door for loading the disk causes the cone thrust arm to come down and the center cone to enter into the disk hole. The center cone catches the inside diameter of the disk and sets it to the correct position. Closing the front door causes the door latch to function and the closed status to be maintained.

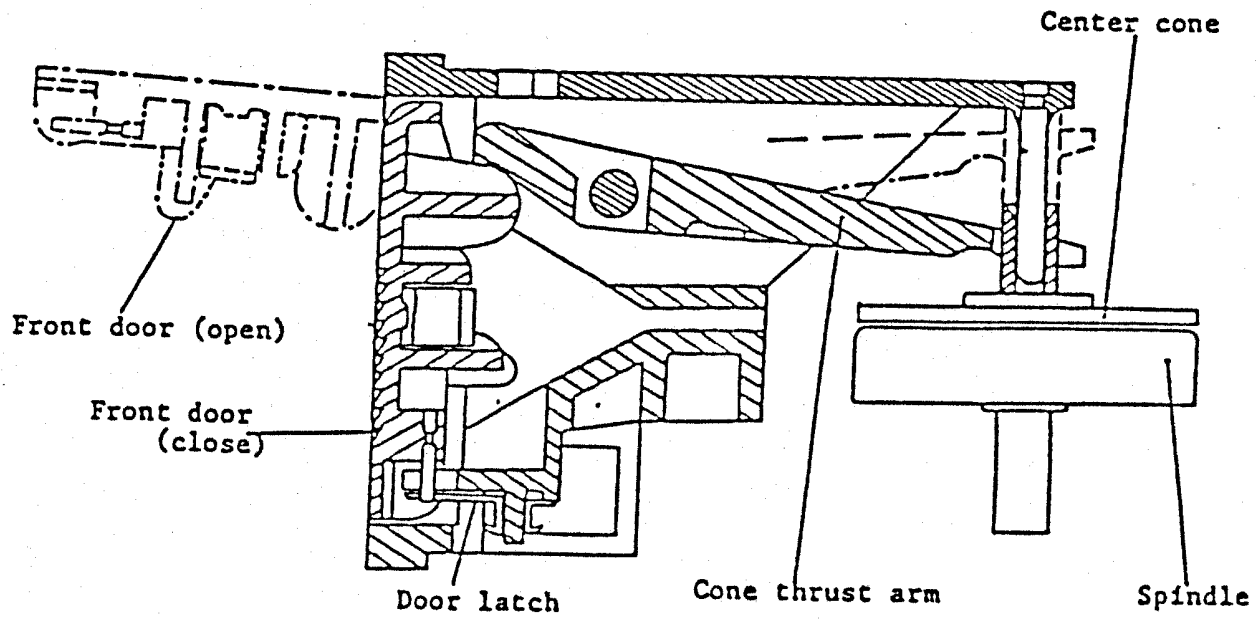


Fig. 3-3 Spindle and front door feature

3.3 Positioning feature

The positioning feature consists of the following parts.

Stepper motor
Pulley
Steel belt
Carriage assembly
Guide bar

The revolution by 3.6° per step of the stepper motor is converted into rectilineal motion by the pulley steel belt feature directly connected to the motor axis and conveyed to the carriage assembly. The carriage assembly consists of the carriage, side 0 R/W head and side 1 R/W head, and loads and unloads the head by the head load feature.

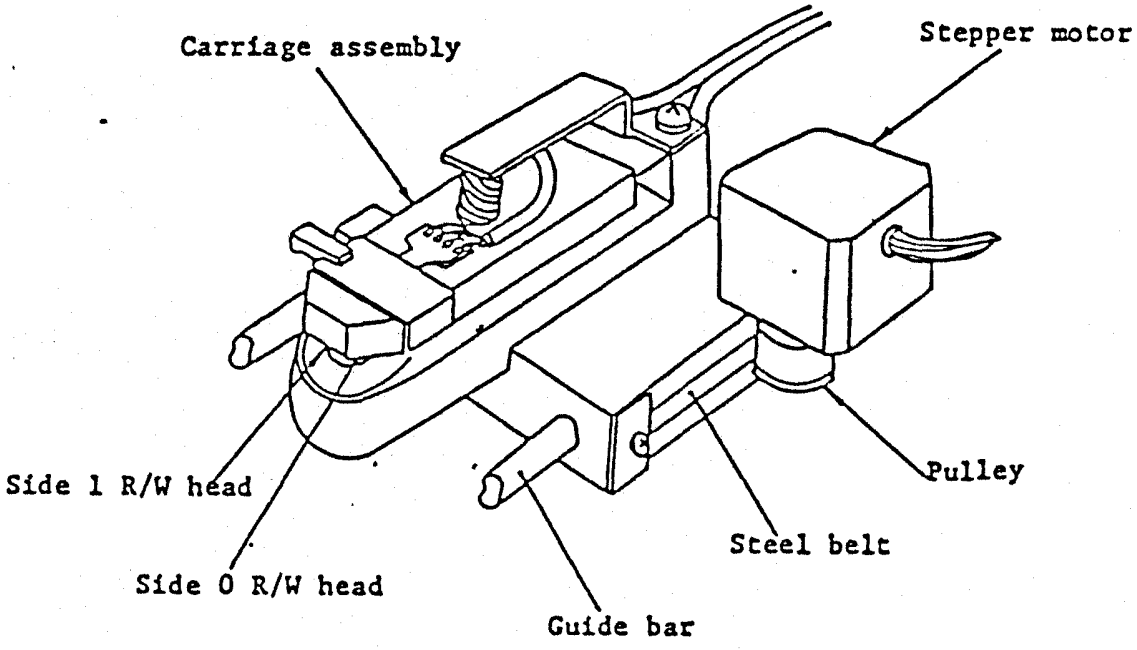


Fig. 3-4 Positioning feature

3.4 Head load feature

The head load feature consists of the following parts.

Solenoid
Head load arm
Stabilizer pad

The solenoid is excited by the HEAD LOAD signal, the head load arm is pressed down and the stabilizer pad presses the disk to prevent the disk from vibrating. Also, the side 1 R/W head is pressed against the disk. Releasing the HEAD LOAD signal causes the stabilizer pad and side 1 R/W head to separate from the disk.

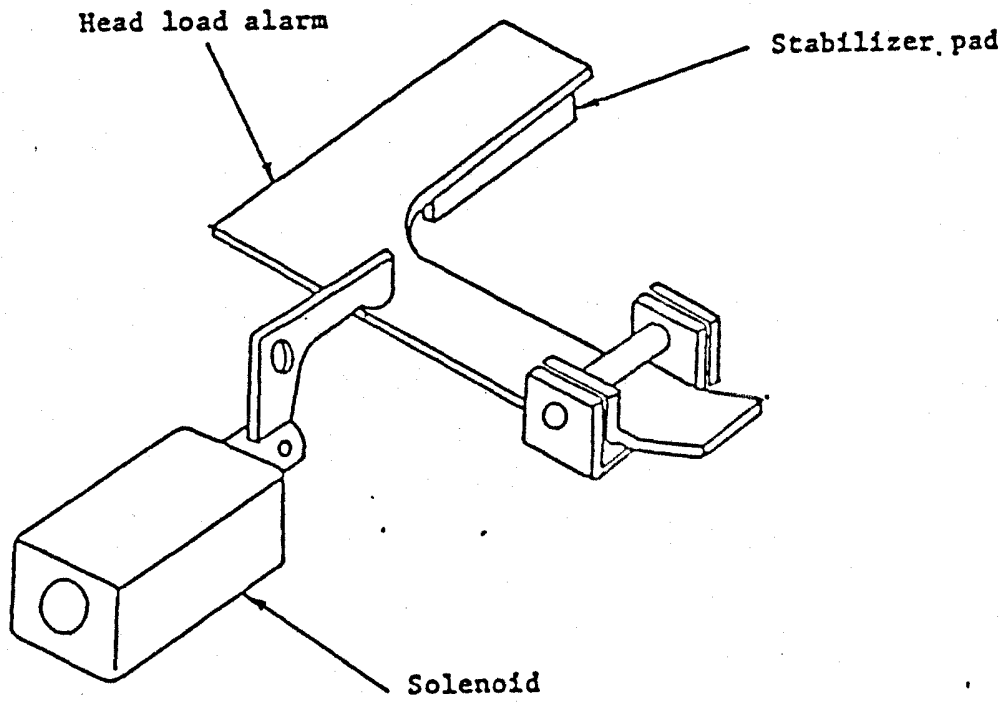


Fig. 3-5 Head load feature

3.5 Circuit

3.5.1 Stepper motor control

The stepper motor is a 4-phase DC motor and the circuit built in the IC MB14036 controls the motor.

The motor makes 3.6° revolutions per STEP signal. The stepper motor revolution is converted into rectilineal motion of the read/write head by a steel belt. The DIRECTION-IN signal regulates the direction of the head towards the inner direction at the low level and towards outer direction (towards track 00) at the high level.

Fig. 3-8 shows the 4-phase status transfer.

The signal timing condition is as follows.

Step signal time interval: Over 6 ms

The DIRECTION-IN signal is required to be determined over 1 µs prior to the STEP signal termination (step start point.)

When the WRITE GATE signal is low during write operation, the STEP signal is invalid.

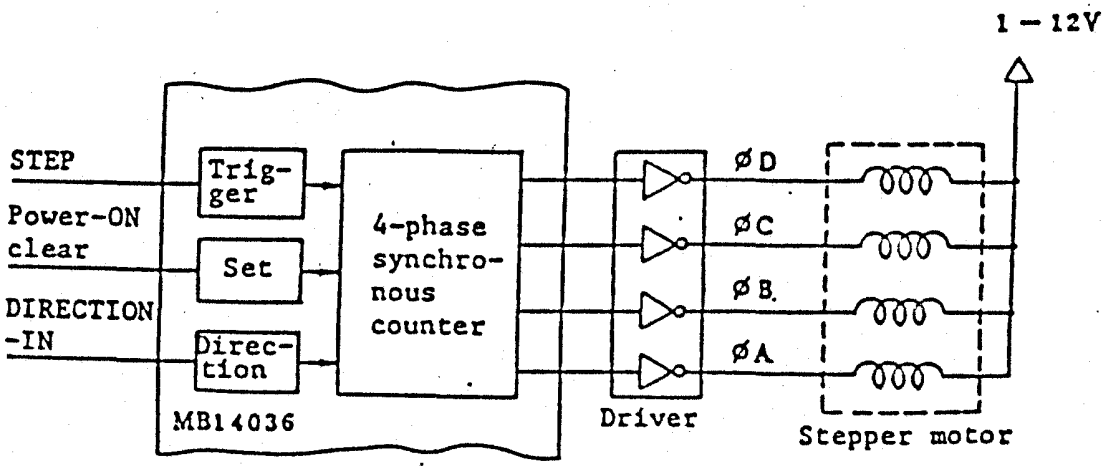


Fig. 3-6 Stepper motor control circuit

3.5.3 Head load circuit and operation confirmation LED

The head load feature is operated by the solenoid. When the disk is revolving at the optimum speed, the head load solenoid is drawn if the HEAD LOAD signal becomes low. The disk revolution is sensed by the index detector. When the solenoid is drawn, transistor T12 is turned ON by one shot of 35 m sec to supply sufficient start current. Transistor 2SC828 is used as the operation confirmation LED DRIVER. This can be operated by the interface signal when the disk's speed is optimum.

The signal is selected by the jumper switch.

When the index hole is positioned between the LED and photo transistor, the LED light reaches the photo transistor, and a positive pulse of 2.5 ms - 5 ms is generated in the comparator output. This falling edge is delayed by one shot, and as a 1.5 - 5 ms pulse, is conveyed to the host system as a negative pulse when the I/O enable signal is active.

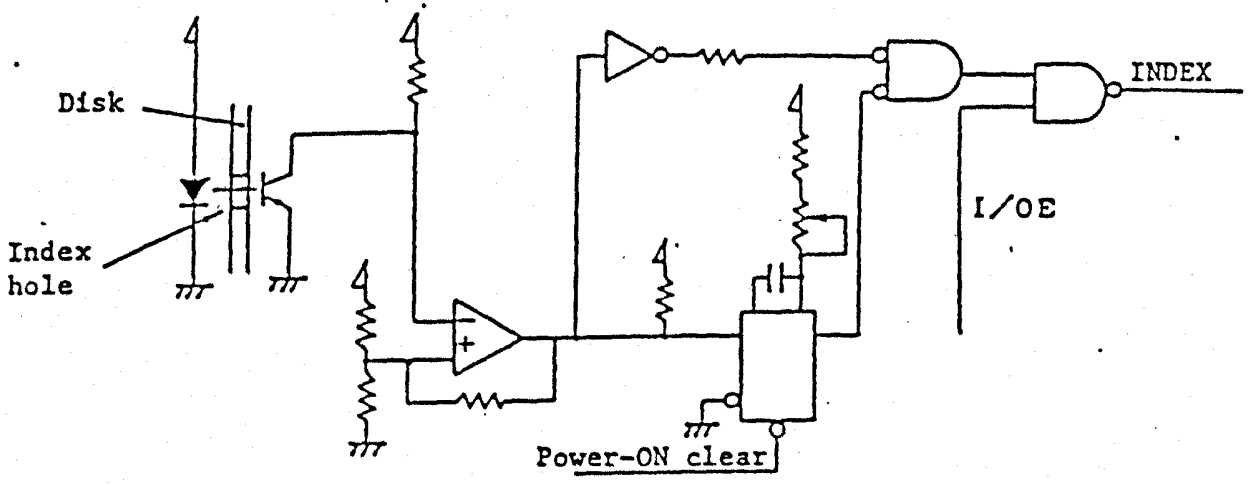


Fig. 3-14 Index detection circuit

Ready detector

The ready detector is provided for monitoring the disk speed by the index pulse and built in the LSI (IC15).

When the index pulse time interval is over 300 ms, the IC15 READY (17-pin) output is low. When it is below 300 ms, the READY output becomes high (active).

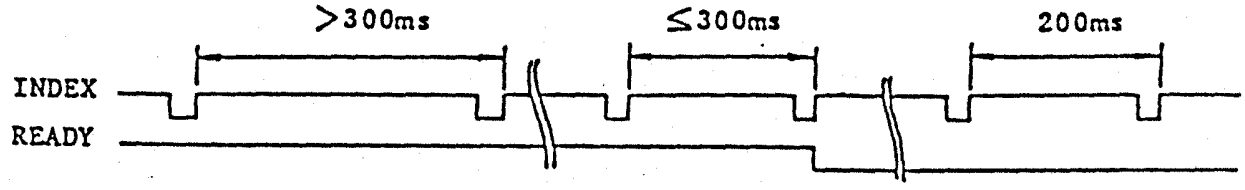


Fig. 3-15 Ready timing

3.5.7 Read/write circuit

Read/write head

The read/write head is a tunnel erase type ceramic head. The head consists of the two read/write coils, one erase coil and three coils. The erase coil is excited in the write mode, and a noise prevention area is formed at both sides of a track recorded by the read/write coil. The two read/write coils are rolled on one core chip and center-tapped. The read/write head connection is illustrated in Fig. 3-17. At the write operation time each bit of write data is alternatively distributed by each coil of the D-FF, and magnetic flux inversion is generated. Writing data on the old data causes the old data to be replaced by the new data.

At the read time the output voltage is inducted when the read/write head gap passes the magnetic flux inversion section. This voltage is sent to the read circuit. The specifications are shown below.

Magnetic inversion density	5876 FCI (inner track) FCI: Flux Changes/Inch			
Read/write frequency (at the head)	FM record	62.5 KHz	125 KHz	
	MFM record	62.5 KHz 125 KHz	83.3 KHz	
Magnetic inversion time	FM record	4 μs	8 μs	
	MFM record	4 μs	6 μs	8 μs
Track interval	0.0208 inches (0.529 mm)			
Track width (before erase)	0.013 inches (0.330 mm)			
(after erase)	0.0124 inches (0.314 mm)			

Receiving data from the host system in this status causes the write flip-flop to turn ON the transistors T06 and T07 alternately. Hence, the write current Iω, Iω' determined by R29 is supplied to the read/write coils ω_1, ω_2 alternately. The inversion magnetic field corresponding to the data is stored in the disk.

When the erase enable signal is low, transistor T08 turns ON, and current I_E is supplied to the erase coil. The current I_E value is determined by resistance R43. The erase enable signal becomes low after the write gate signal has become low and a fixed delay time has elapsed. The reason is that the tunnel erase gap is positioned by being preceded by the read/write gap. Fig. 3-21 shows the erase ready circuit.

The write current and erase current are cut by the DC control circuit if an electrical trouble occurs.

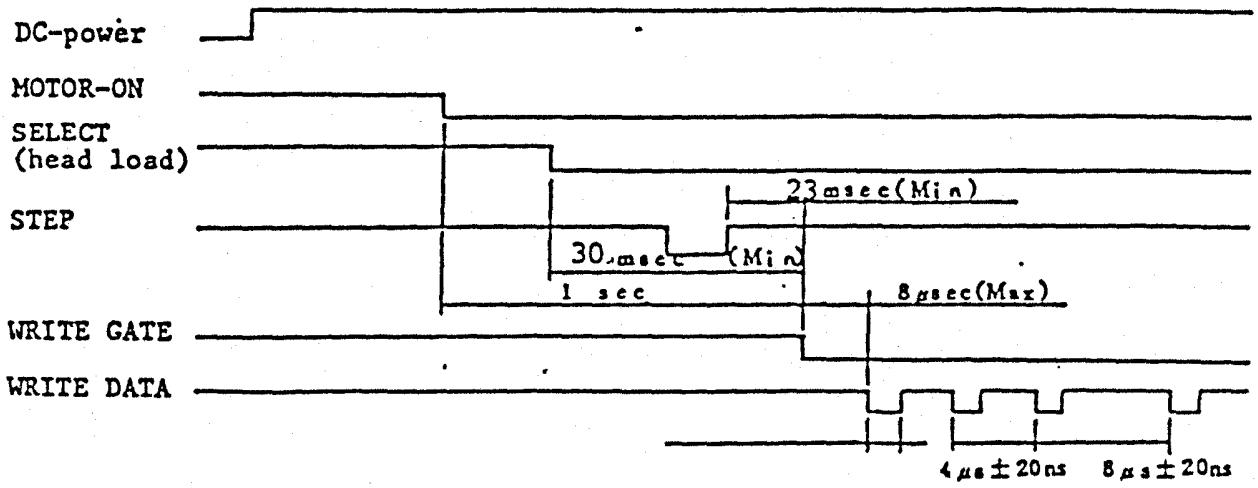


Fig. 3-18 Write start timing

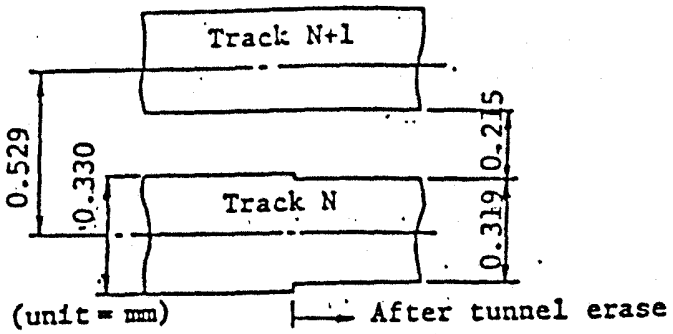


Fig. 3-16 Track dimension

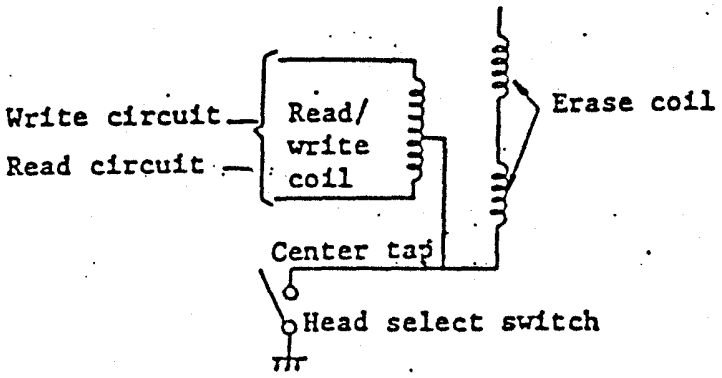


Fig. 3-17 Read/write head connection diagram

Write circuit

The write circuit converts the serial data passed from the host system into the magnetic pattern on the disk. Fig. 3-18 shows the write timing.

Fig. 3-19 shows a simplified write circuit. Loading the head and making the WRITE GATE signal become low causes the drive to enter into the writable status.

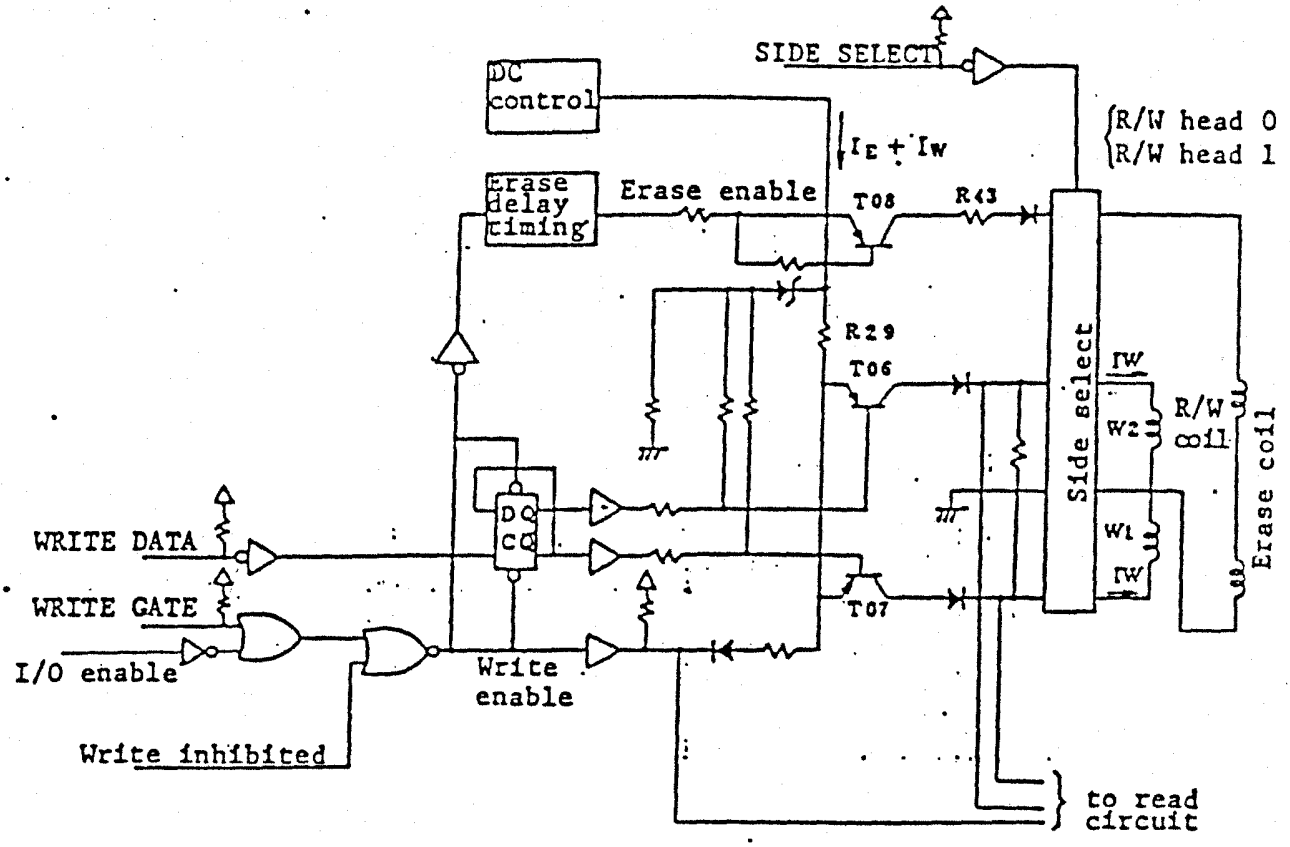


Fig. 3-19 Write circuit

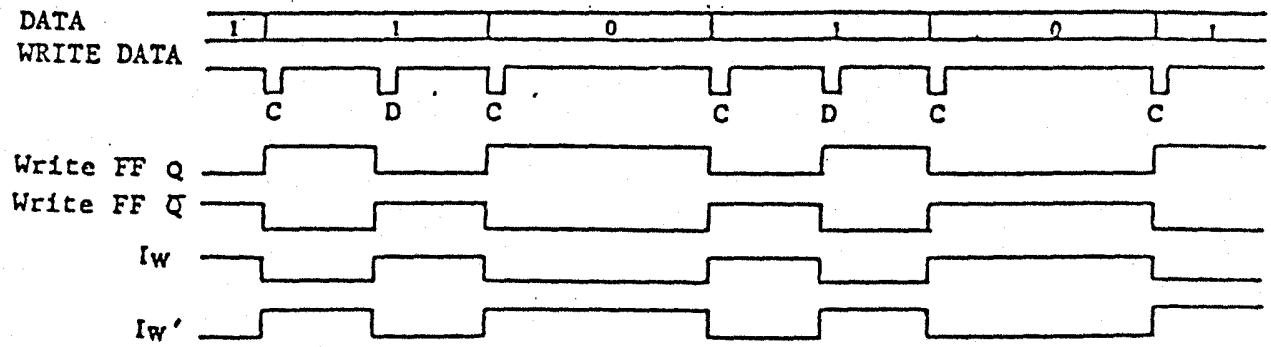


Fig. 3-20 Write timing

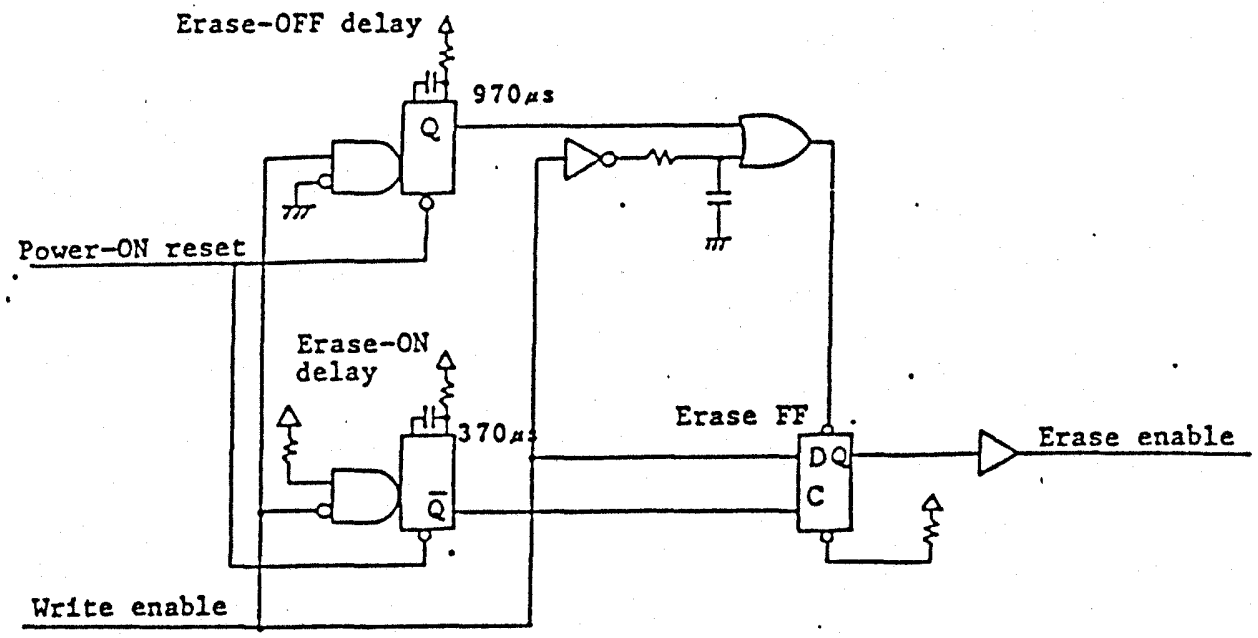


Fig. 3-21 Erase delay circuit

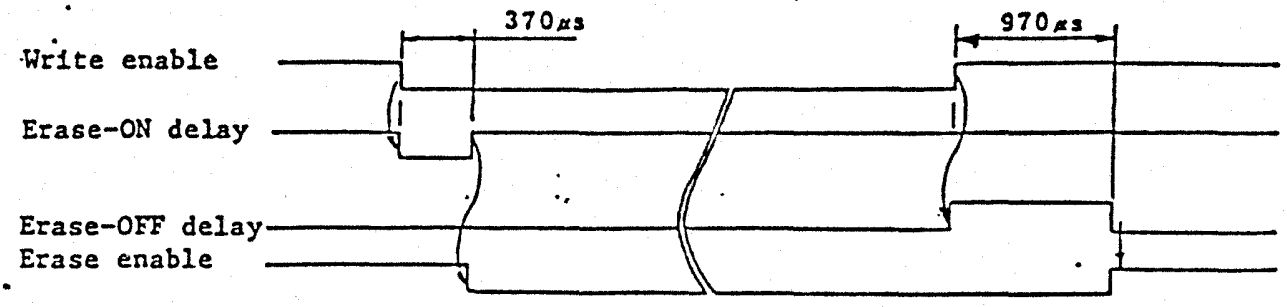


Fig. 3-22 Erase delay timing

Read circuit

Data stored in the disk are regenerated by the read circuit. Fig. 3-29 shows the read timing.

Fig. 3-23 shows the read circuit. Loading the head and making the WRITE GATE signal become high causes the drive to enter into readable status. The read circuit consists of IC MC3470 and necessary external parts.

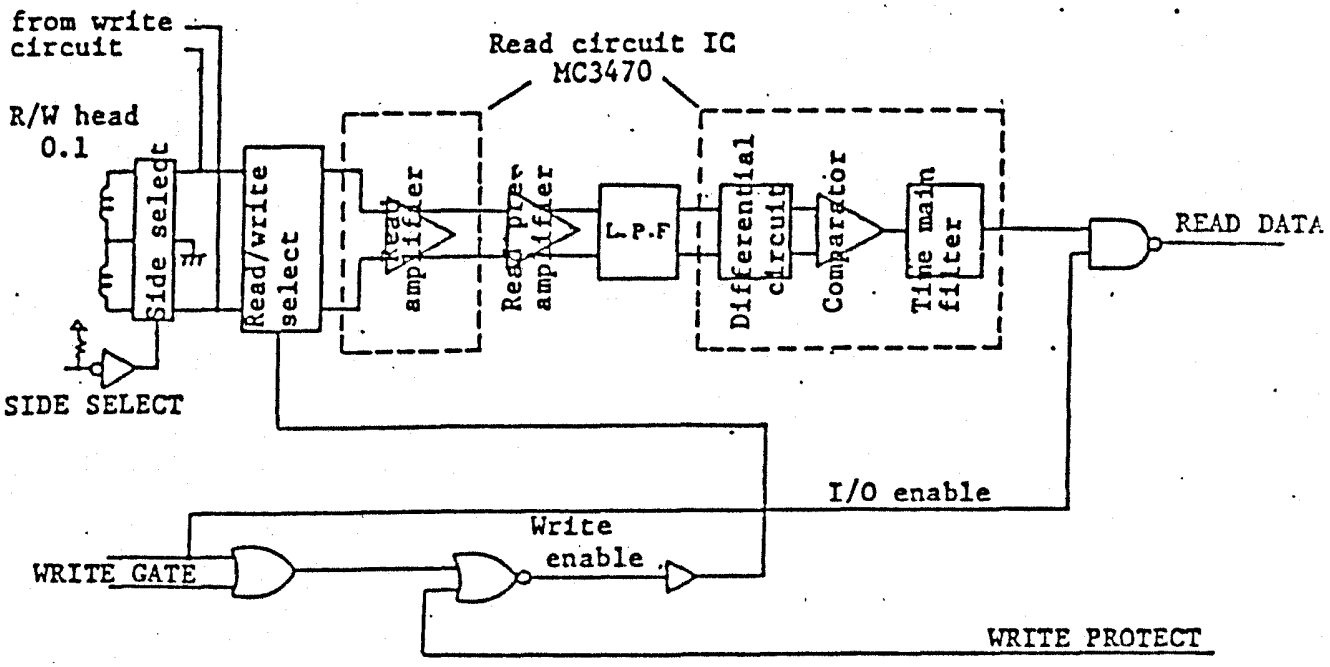


Fig. 3-23 Read circuit

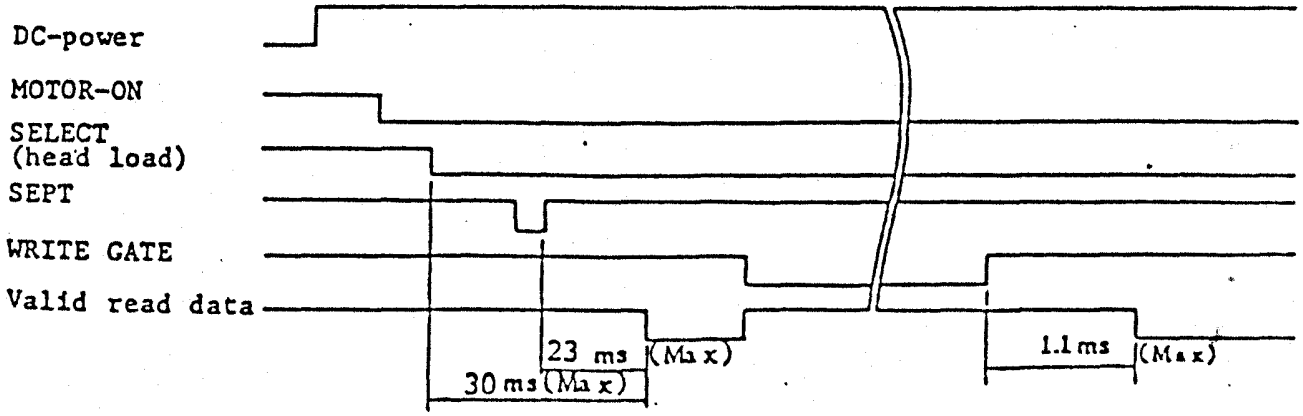


Fig. 3-24 Read start timing

Read/write select

The read/write select circuit consists of two MOS-EET switches. The input side of the switch is connected to the coil of the read/write head, and the output side to the read amplifier.

When the drive is in write mode the write enable: 01 signal turns OFF transistors T01 and T02 at the high level. In read mode the write enable: 01 signal turns ON transistors T01 and T02 at the low level. The read/write head and the read amplifier are connected.

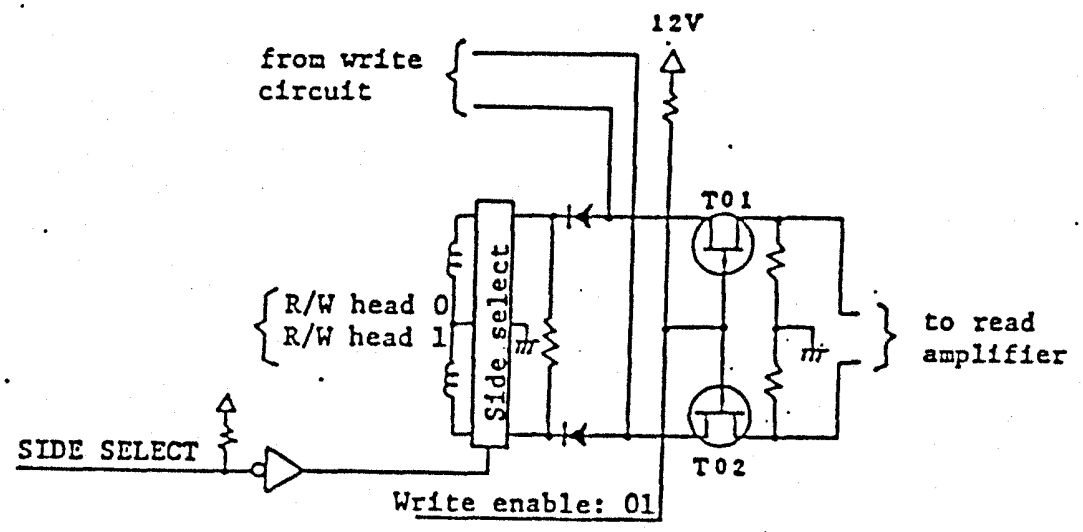


Fig. 3-25 Read/write circuit

Read amplifier circuit and filter network

The read signal is amplified by the high performance linear amplifier comprising the MC3470 preamplifier and transistor. The read signal amplified by both amplifiers drives the next filter network. The filter network is a low-pass filter.

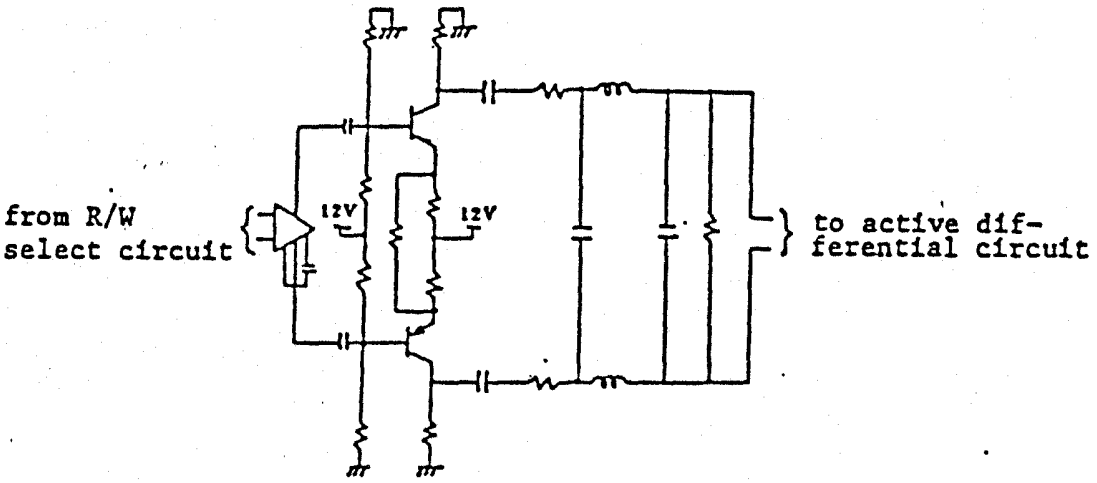


Fig. 3-26 Read amplifier circuit and filter network

Active differential circuit and comparator

Both circuits are part of the MC3470. Fig. 3-27 shows the outline. The active differential circuit is a differential amplifier, the emitter of which is coupled by the capacitor. The current passing through the capacitor becomes the differentiation of the input voltage. In short, the current passing to the collector resistance is the differentiated input voltage. Hence, the output voltage Vo of the differential amplifier is also the differentiated input voltage.

$$Ic = C \frac{dVin}{dt}$$

$$Vo = 2RIc = 2RC \frac{dVin}{dt}$$

The output voltage Vo is inputted into the connector which detects the zero-cross. As a result, the peak of the voltage inputted into the differential circuit is detected. Fig. 3-29 shows the timing of the differential circuit and comparator.

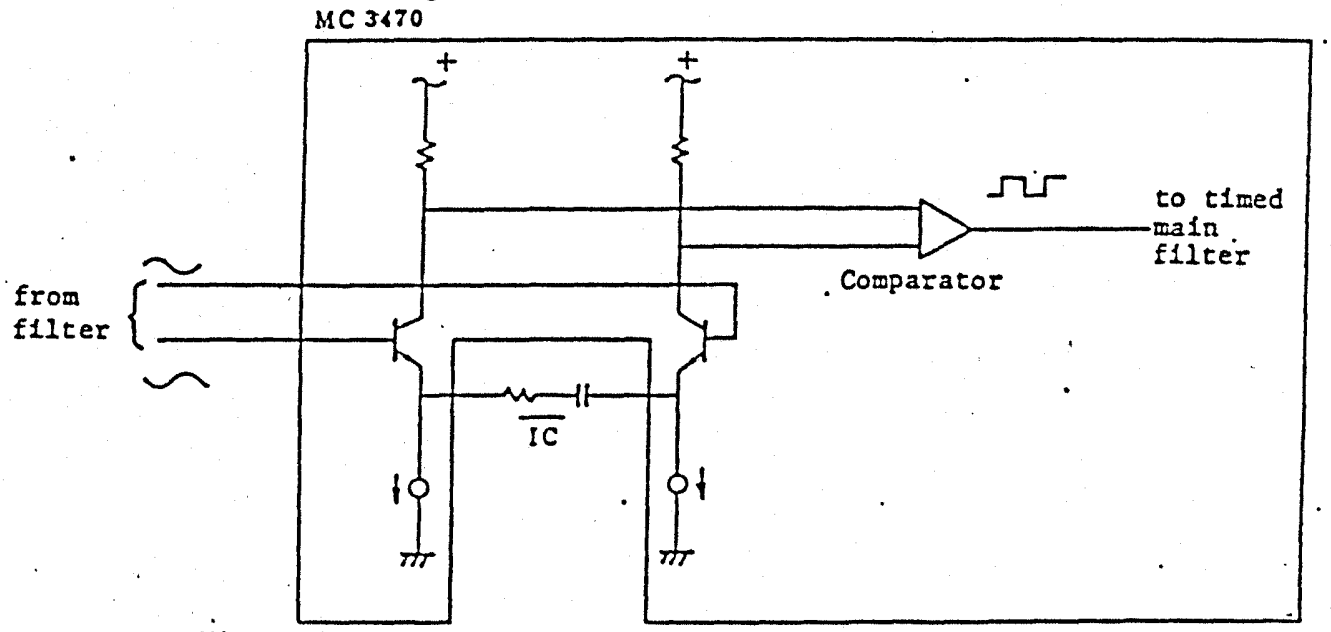


Fig. 3-27 Active differential circuit and comparator

Timed main filter and crossover detector

Both circuits are part of the MC3470. The timing filter removes an erroneous crossover of the comparator caused by shouldering of the differentiated read signal. When a high resolution head is used, shouldering sometimes occurs in the outer circumference of the drive.

The timed main filter consists of a pulse generator, timed main one shot and timed main flip-flop. The pulse generator generates a short pulse to trigger the timed main one shot at every input transfer. The timed main one shot pulse width is determined by the external resistance and capacitor value.

The MDD is set to 2.5 μs. The information passed from the comparator is delayed by 2.5 μs by the timed main one-shot and loaded on the timed main flip-flop. Even if the timed flip-flop is clocked by an erroneous crossover, the timed main flip-flop output does not change, because the erroneous crossover time is shorter than 2 μs.

The crossover detector is triggered at the every timed main flip-flop transfer. The pulse width of the crossover detector is determined by the external resistance and capacitor value, and is set to 500 n.sec.

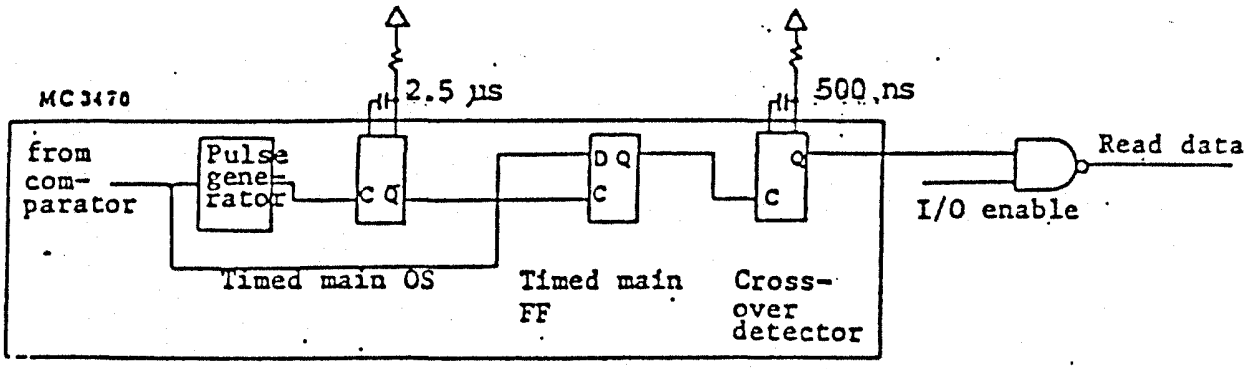


Fig. 3-28 Timed main filter and crossover detector

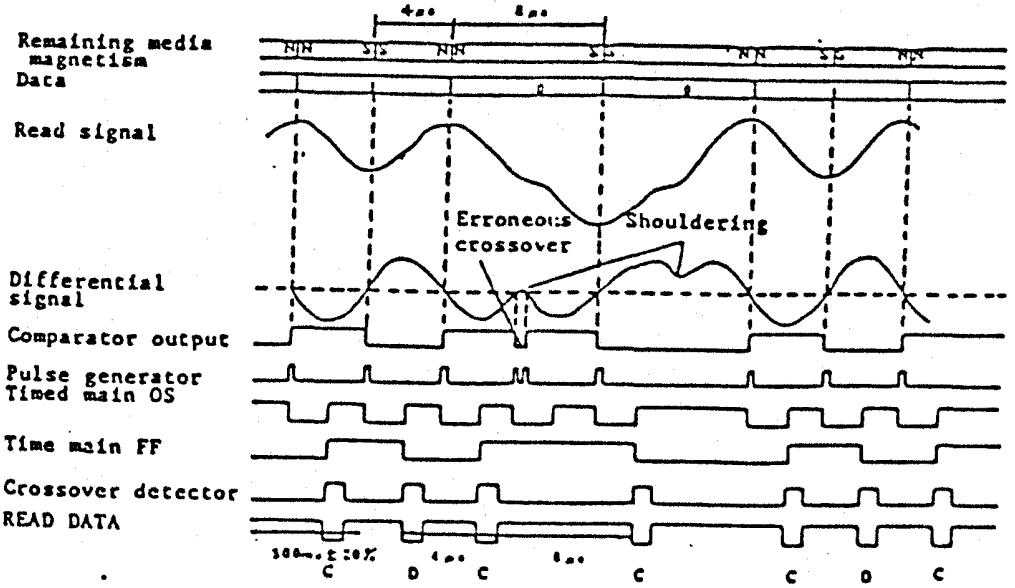


Fig. 3-29 Read timing

3.5.8 DC control circuit and power-ON reset circuit

DC control circuit .

Fig. 3-30 shows the DC control circuit. This circuit is used to monitor the DC 5V and DC 12V power voltage. When it deviates from the following limits, the write current and erase current are not secured.

5V DC < 4.3V

12V DC < 8.1V

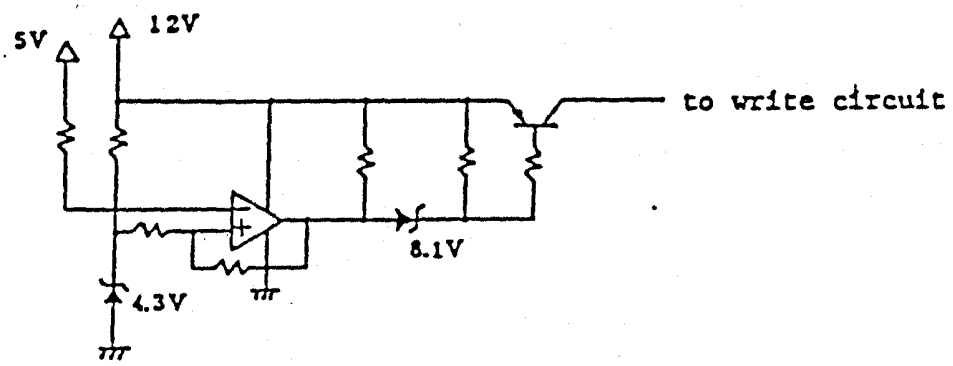


Fig. 3-30 DC control circuit

Power-ON circuit

Fig. 3-31 shows the power-ON reset circuit. When the power is turned on, capacitor C19 begins charging to 3V. When the capacitor C1 voltage is lower than the buffer threshold voltage, the power-ON reset signal becomes low. Hence, the initial reset pulse of 40 m sec can be generated.

The power-ON reset pulse resets the following circuits.

- o Erase-OFF delay one shot
- o Ready detection
- o Step one shot

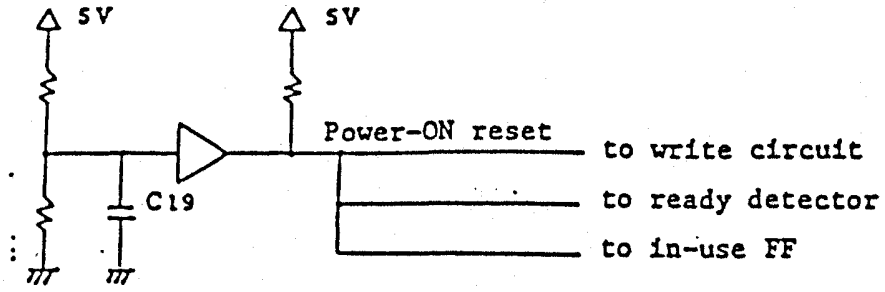


Fig. 3-31 Power-ON reset circuit

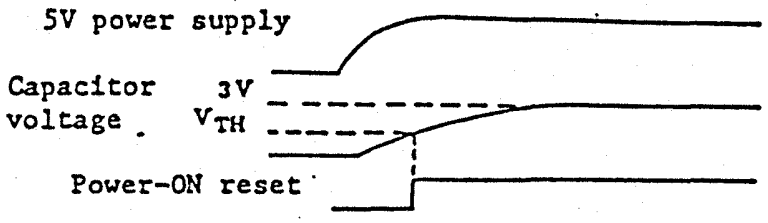
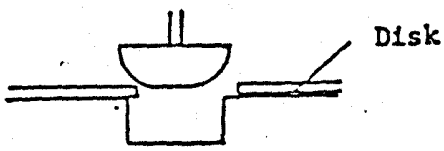


Fig. 3-32 Power-ON reset timing

3.5.9 Fine clamp feature

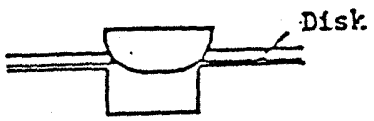
This feature prevents the disk center hole from being damaged at the clamp time by revolving and clamping the disk to enhance the centering precision. It consists of the switch feature and motor-ON timer circuit.

a) without fine clamp



Imprecise disk insertion can result in damage to the disk center hole.

b) with fine clamp



The disk center hole can be determined accurately by revolving the disk.

Fig. 3-33 Fine clamp operation

The MDD operates the clamp by being connected to the front door. (see 3.2) The disk is revolved at the clamp time by the motor which runs for about 3 sec when the micro switch is turned ON by the front door motion.

The fine clamp feature timing, switch feature and motor-ON timer circuit are shown below.

Door status

Fine clamp motor-ON

Clamp status

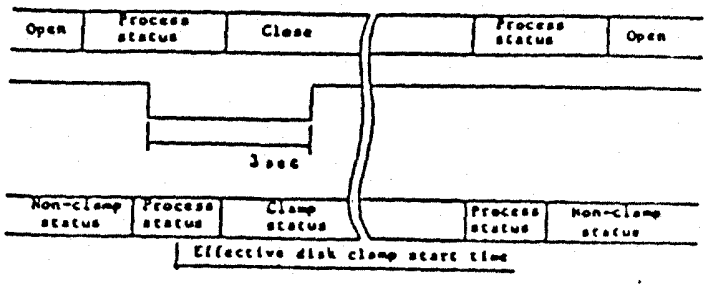


Fig. 3-34 Fine clamp feature timing

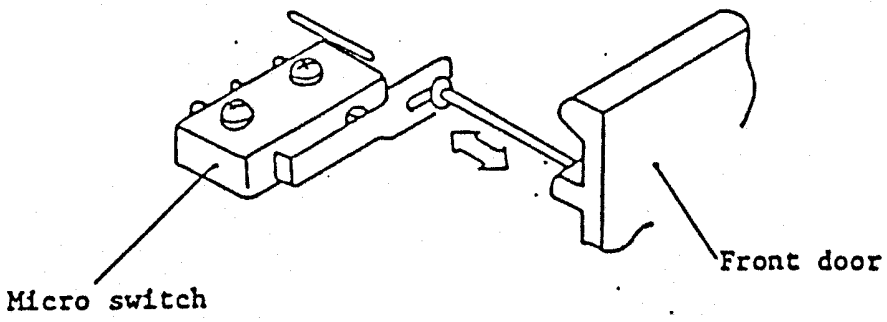


Fig. 3-35 Fine clamp switch feature

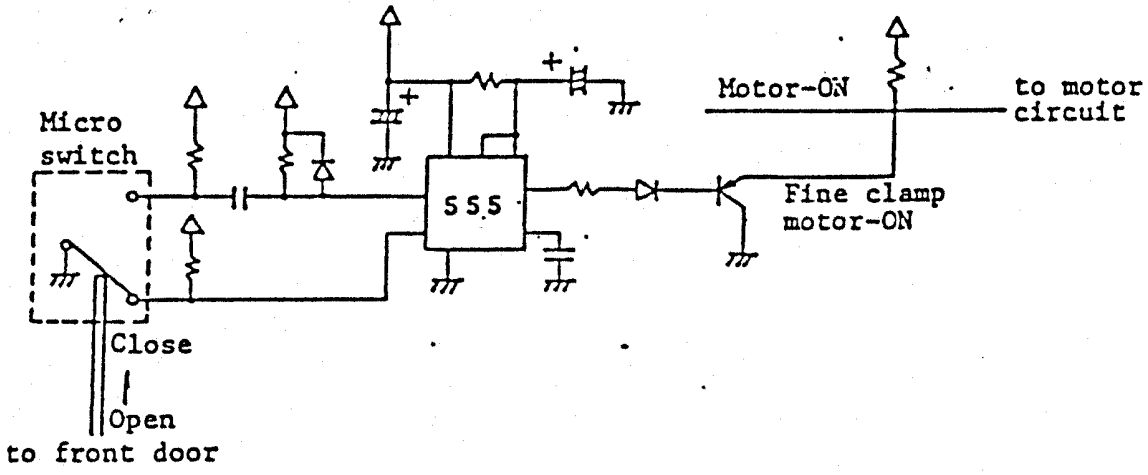
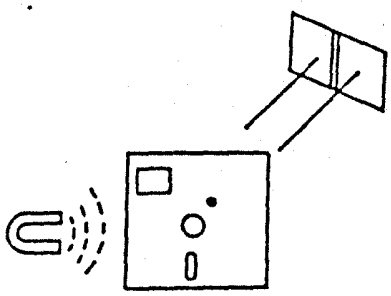


Fig. 3-36 Fine clamp motor-ON timer circuit

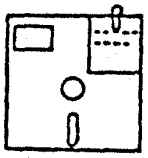
4. Handling Mini Floppy Disks

The following are the precautions to be observed when handling mini floppy disks.

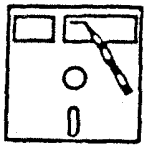
[Unsatisfactory]



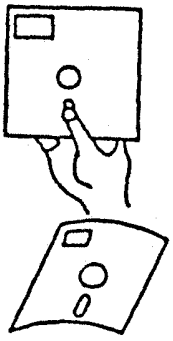
- o Do not expose disks to direct sunlight or place them near a source of heat.
- o Do not place disks in a place which is subject to the influence of a magnetic field.



- o Do not expose disks to cigarette smoke.
- o Do not put clips or rubber bands on disks.

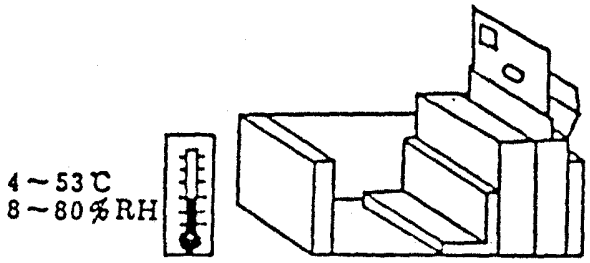


- o Do not write directly on disks using a pen or pencil.

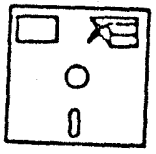


- o Do not touch the recording face of disks (oblong hole portion).
- o Do not bend or fold disks.

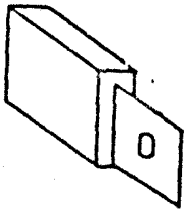
[Satisfactory]



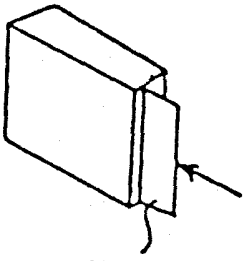
- o Store disks in a clean environment at suitable temperature and humidity.
- o When not using a disk, insert it in an envelope, then insert the envelope in a special-purpose case, and store it vertically.



- o Paste labels on disks after writing on them first.

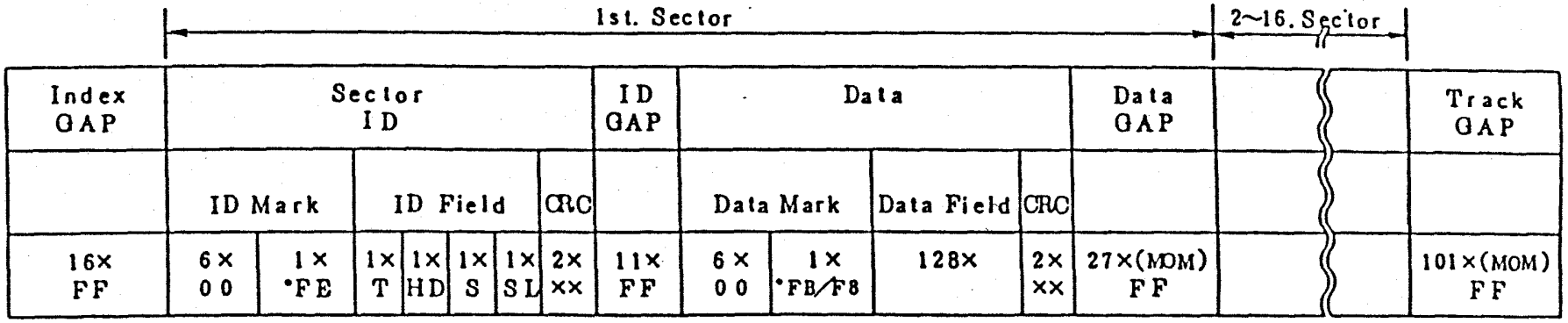


- o Before using a disk, it is recommended that it be left for a suitable time in the same environment as the drive in order to acclimatize it.

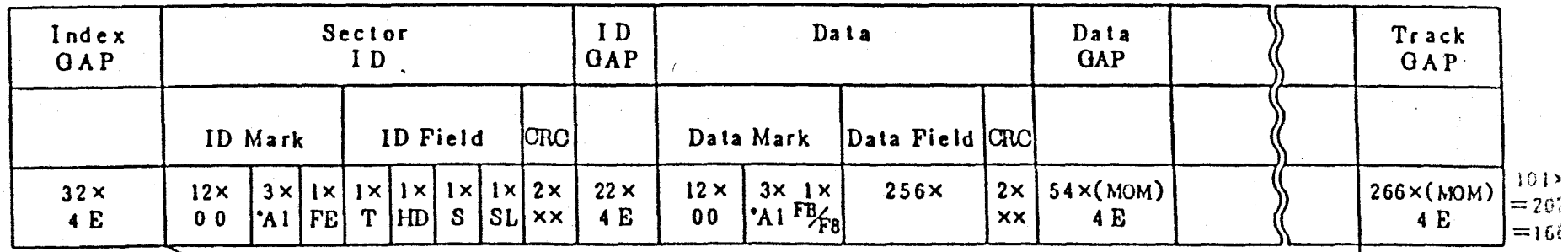


- o Completely insert the media to the back of the drive before closing the door.

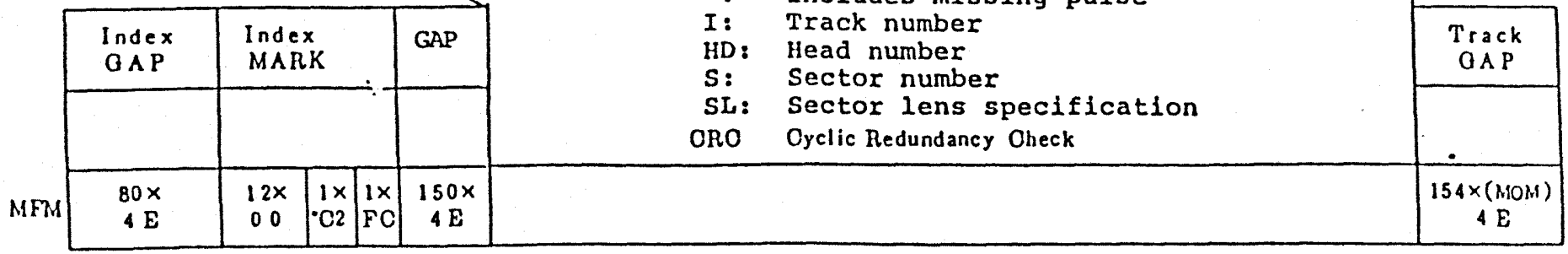
Format example 1 (FM, 16 sectors, 128 bytes, conformance to ISO)



Format example 2 (MFM, 16 sectors, 256 bytes, conformance to ISO)



Format example 3 (MFM, 16 sectors, 256 bytes, conformance to IBM)



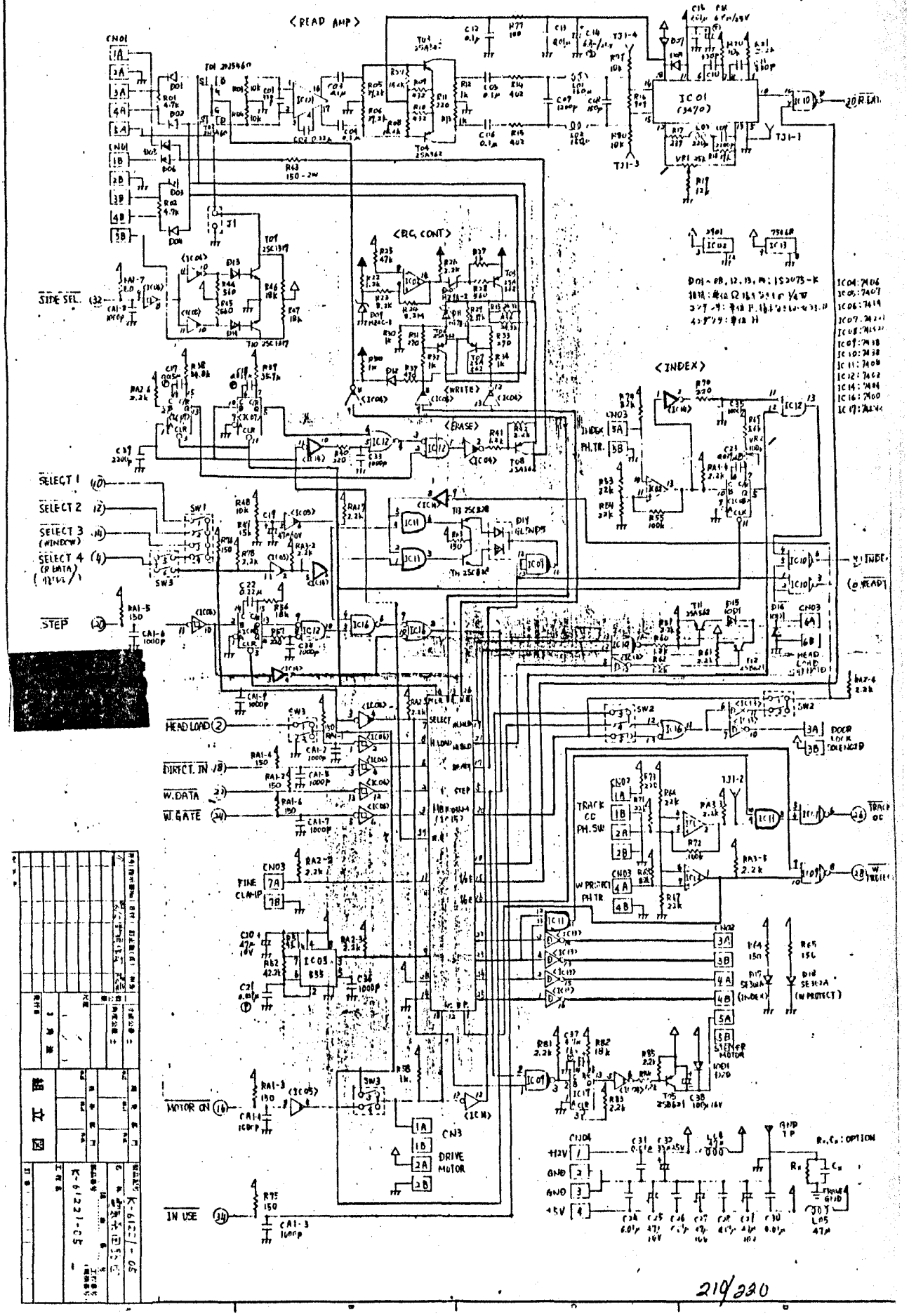
*: Includes missing pulse
I: Track number
HD: Head number
S: Sector number
SL: Sector lens specification
CRC Cyclic Redundancy Check

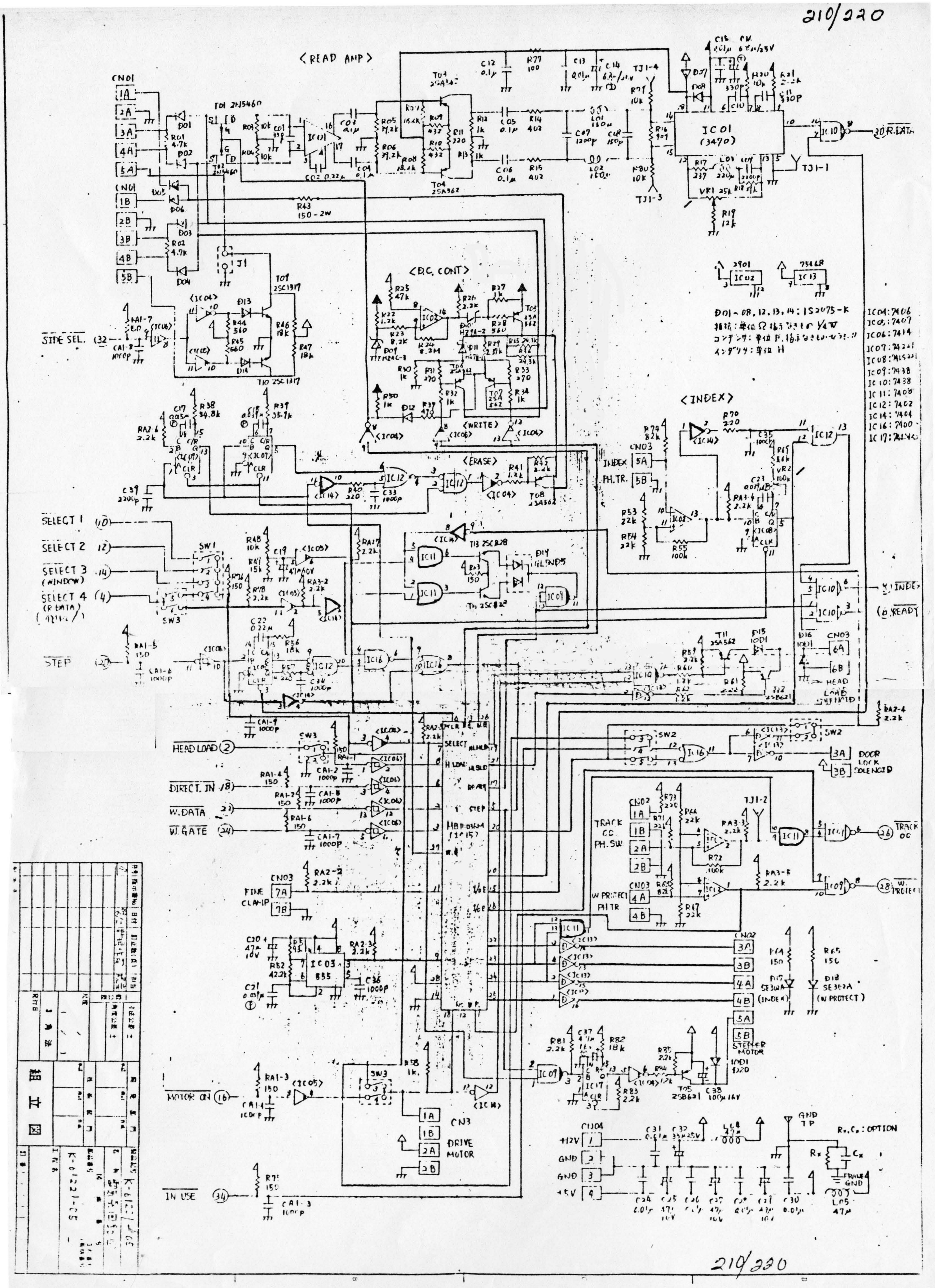
ss'y parts

N	KEY NO	PART NO	Q'TY	DESCRIPTION	REMARKS
*		SY7-5051-000	1	MICRO SWITCH ASS'Y	
*		SY7-5052-000	1	PHOTO TRANSISTOR ASS'Y, WRITE PROTECT	
*		SY7-5053-000	1	PHOTO TRANSISTOR ASS'Y, INDEX	
*		SY7-5054-000	1	PHOTO COUPLER ASS'Y	
*		SY7-5055-000	1	STEPPING MOTOR ASS'Y	
*		SY7-5056-000	1	MAIN PCB ASS'Y	
*		SY7-5057-000	1	HEAD LOAD ARM & SOLENOID ASS'Y	
*		SY7-5058-000	1	FRONT DOOR ASS'Y	
*		SY7-5059-000	1	0-1 HEAD ASS'Y	
*		SY7-5060-000	1	STEEL BELT	
*		SY7-5061-000	1	DD MOTOR ASS'Y	
*		SY7-5081-000	1	PLATE, SPRING	
*		SY7-5082-000	1	SPRING, DOOR	
*		SY7-5083-000	1	SPRING, HEAD LOAD	
*		SY7-5084-000	2	HOLDER, STEEL BELT (A)	
*		SY7-5085-000	1	HOLDER, STEEL BELT (B)	

MAIN PCB ASS' Y

N	KEY NO	PART NO	Q'TY	DESCRIPTION	REMARKS
*	D01 ~08	SY7-5074-000	8	DIODE 1S2075-K	
*	D09	SY7-5075-000	1	ZENER DIODE HZ4C-3	
*	D10	SY7-5077-000	1	ZENER DIODE HZ9A-2	
*	D11	SY7-5076-000	1	ZENER DIODE HZ7B-1	
*	D12 ~14	SY7-5074-000	3	DIODE 1S2075-K	
*	D15,16	WA1-0137-000	2	DIODE 10D1	
*	D17,18	WG1-0091-000	2	LED SE302A	
*	D19	SY7-5078-000	1	LED GL-5ND5	
*	D20	WA1-0137-000	1	DIODE 10D1	
*	IC01	SY7-5065-000	1	IC MC3470	
*	IC02	SY7-5064-000	1	IC HA17901P	
*	IC03	SY7-5086-000	1	IC HA17555PS	
	IC04	X65-7160-000	1	TTL IC SN7406P (HD7406P)	
	IC05	X65-7336-000	1	TTL IC SN7407P (HD7407P)	
	IC06	X65-7448-000	1	TTL IC SN7414P (HD7414P)	
*	IC07	X65-7463-000	1	TTL IC SN74221P (HD74221P)	
*	IC08	WA3-0582-000	1	TTL IC SN74LS221N	
	IC09,10	X65-7301-000	2	TTL IC SN7438P (HD7438P)	
	IC11	X65-7161-000	1	TTL IC SN7408P (HD7408P)	
	IC12	X65-7159-000	1	TTL IC SN7402P (HD7402P)	
*	IC13	SY7-5067-000	1	IC ULN2003A	
	IC14	X65-7142-000	1	TTL IC SN7404P (HD7404P)	
*	IC15	SY7-5066-000	1	IC MB14036M	
	IC16	X65-7011-000	1	TTL IC SN7400P (HD7400P)	
	IC17	WA3-0254-000	1	TTL IC SN74LS123P (HD74LS123P)	
*	L01,02	SY7-5071-000	2	CHOKE COIL 150UH	
*	L03	SY7-5072-000	1	CHOKE COIL 220UH	
*	L04,05	SY7-5073-000	2	CHOKE COIL 47UH	
*	SW1	SY7-5068-000	1	SWITCH B-4A	
*	SW2	SY7-5069-000	1	SWITCH B-5A	
*	SW3	SY7-5070-000	1	SWITCH B-6A	
*	T01,02	SY7-5079-000	2	TRANSISTOR 2N5460 (FET)	
*	T03 ~08	WA2-0257-000	6	TRANSISTOR 2SA562TM-Y	
	T09,10	WA2-0189-000	2	TRANSISTOR 2SC1317-R	
*	T11	WA2-0257-000	1	TRANSISTOR 2SA562TM-Y	
*	T12	SY7-5080-000	1	TRANSISTOR 2SB621	
	T13,14	X65-6318-000	2	TRANSISTOR 2SC828	
*	T15	SY7-5080-000	1	TRANSISTOR 2SB621	


<READ AMP>
<BIG CONT>
<INDEX>
<ERASE>
<WRITE>
IC01 (3470)
SIDE SEL.
SELECT 1
SELECT 2
SELECT 3 (WINDOW)
SELECT 4 (P DATA)
STEP
HEAD LOAD
DIRECT. IN
W. DATA
W. GATE
MOTOR ON
IN USE
INDEX
PH. TR.
TRACK 00 PH. SW
W PROTECT PH TR
DOOR LOCK SOLENOID
HEAD LOAD SOLENOID
STEPPING MOTOR
DRIVE MOTOR
+12V
GND
+5V
R.C.: OPTION



210/220
<READ AMP>
<D.C. CONT>
<WRITE>
<ERASE>
<INDEX>
IC01 (3470)
CN01
T01 2N5460
T02 2N5460
T04 2SA562
T09 2SC1317
T10 2SC1317
T08 2SA562
T13 2SC828
T11 2SA562
T12 2SB621
T05 2SB621
R43 150-2W
SIDE SEL. (32
SELECT 1 (10
SELECT 2 (12
SELECT 3 (14 (WINDOW)
SELECT 4 (4 (R DATA)
STEP (20
HEAD LOAD (2
DIRECT. IN (18
W.DATA (22
W.GATE (24
FINE CLAMP
MOTOR ON (16
IN USE (34
30 R.DATA
8 INDEX
(6 READY
26 TRACK OC
28 W. PROTECT
DOOR LOCK SOLENOID
HEAD LOAD SOLENOID
TRACK OO PH.SW.
W PROTECT PH.TR.
INDEX
PH.TR.
DRIVE MOTOR
STEPPER MOTOR
SW1
SW2
SW3
IC03 555
MB11O14M (IC15)
SELECT
H LOAD
READY
STEP
W.E
1/0 E
W.P.
D17 SE303A (INDEX)
D18 SE303A (W PROTECT)
CN04
+12V
GND
GND
+5V
GND TP
Rx, Cx : OPTION
FRAME GND
L05 47μ
D01~08, 12, 13, 14 : 1S2075-K
抵抗：単位Ω 指示なきものは 1/4W
コンデンサ：単位 F. 指示なきものはセラミック
インダクタ：単位 H
2901 IC02
75468 IC13
IC04:7406
IC05:7407
IC06:7414
IC07:74221
IC08:74LS221
IC09:7438
IC10:7438
IC11:7408
IC12:7402
IC14:7404
IC16:7400
IC17:74LS123
組立図
K-6121-C5
210/220